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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/780,586	02/19/2004	Takashi Takamura	118394	2499

25944 7590 07/27/2005

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EXAMINER	
GEBREMARIAM, SAMUEL A	
ART UNIT	**PAPER NUMBER**
2811	

DATE MAILED: 07/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/780,586	TAKAMURA, TAKASHI	
	Examiner	Art Unit	
	Samuel A. Gebremariam	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Double Patenting

1. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

2. Claims 1-6 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 of U.S. Patent No. 6,914,228 in view of Miida US patent No. 6,051,857. Although the conflicting claims are not identical, the claimed subject matter of the instant application claimed invention is not patentably distinct from each other because of the following reasons:

The claimed subject matter of the instant application, i.e., "a solid-state imaging device, comprising: a pixel array having a plurality of unit pixels, each unit pixel including a photodiode and an insulated gate field effect transistor that detects a photocharge; the photo diode and the insulated gate field effect transistor sharing a well region of a first conductivity type that is formed in a semiconductor layer of a second conductivity type, the semiconductor layer of the second conductivity type formed on a semiconductor substrate of the first conductivity type; the insulated gate field effect

transistor comprising: a source diffused region of the second conductivity type formed on a surface of the well region; a drain diffused region of the second conductivity type formed on the semiconductor layer; a gate electrode formed over the well region between the drain diffused region and the source diffused region with a gate insulating film therebetween; a channel region formed in the surface of the well region under the gate electrode and having an impurity layer of the second conductivity type; and a heavily doped buried layer of the first conductivity type formed under the channel region in the well region and near the source diffused region, having an impurity concentration higher than that of the well region, and being an accumulation region that accumulates a charge of a given conductivity type generated in response to light incident on the photo diode; and the control circuit being configured to apply predetermined voltage to the source diffused region and the gate electrode, respectively, by which the channel region is brought into a conductive state, so as to bias a junction region formed of the semiconductor substrate and the semiconductor layer in a forward direction, and the control circuit accumulates a predetermined amount of the charge of a predetermined conductivity type in the accumulation region thereby, and thereafter, discharges the charge of a predetermined conductivity type accumulated in the accumulation region" as recited in claim 1 is already claimed in claim 1 of US patent 6,914,228.

Claim 1 of patent No. 6,914,228 discloses the claimed structure except for the limitation of "a control circuit that controls an operation of the pixel array the control circuit including a voltage generating circuit a vertical control circuit and a horizontal control circuit the control circuit configured to be capable of discharging a charge in the

insulated gate field effect transistor by applying a gate voltage and a source voltage to the insulated gate field effect transistor via the vertical and horizontal control circuits".

It is conventional and also taught by Miida (fig. 7A) forming a control circuit (fig. 7A) that controls an operation of the pixel array the control circuit including a voltage generating circuit,a vertical control circuit (102) and a horizontal control circuit (104) the control circuit configured to be capable of discharging a charge in the insulated gate field effect transistor by applying a gate voltage and a source voltage to the insulated gate field effect transistor via the vertical and horizontal control circuits.

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the control circuit that controls an operation of the pixel array the control circuit including a voltage generating circuit a vertical control circuit and a horizontal control circuit the control circuit configured to be capable of discharging a charge in the insulated gate field effect transistor by applying a gate voltage and a source voltage to the insulated gate field effect transistor via the vertical and horizontal control circuits taught by Miida in the structure of patent No. 6,914,228 in order to form an integrated solid-state imaging device.

Furthermore the claimed limitations of claims 2-4 are within the scope of the claimed limitations of claims 1-7 of US patent 6,914,228.

Conclusion

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Samuel A. Gebremariam whose telephone number is (571)-272-1653. The examiner can normally be reached on 8:00am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's acting supervisor, Steve Loke can be reached on (571) 272-1657. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SAG
July 17, 2005